



US008251707B2

(12) **United States Patent**
Panella et al.

(10) **Patent No.:** **US 8,251,707 B2**
(45) **Date of Patent:** **Aug. 28, 2012**

(54) **PATCH PANEL ASSEMBLY FOR USE WITH DATA NETWORKS**

(75) Inventors: **Augusto P. Panella**, Naperville, IL (US);
Elliot A. Baines, Naperville, IL (US);
Jeng-De Lin, Yorkville, IL (US)

(73) Assignee: **Molex Incorporated**, Lisle, IL (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/123,036**

(22) PCT Filed: **Oct. 7, 2009**

(86) PCT No.: **PCT/US2009/059807**

§ 371 (c)(1),
(2), (4) Date: **Jun. 28, 2011**

(87) PCT Pub. No.: **WO2010/042593**

PCT Pub. Date: **Apr. 15, 2010**

(65) **Prior Publication Data**

US 2011/0256738 A1 Oct. 20, 2011

Related U.S. Application Data

(60) Provisional application No. 61/103,487, filed on Oct. 7, 2008, provisional application No. 61/103,532, filed on Oct. 7, 2008.

(51) **Int. Cl.**
H01R 29/00 (2006.01)

(52) **U.S. Cl.** **439/49; 439/76.1**

(58) **Field of Classification Search** **439/49,**
439/76.1, 540.1

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,305,987 B1 10/2001 Crane, Jr. et al.
7,207,846 B2 4/2007 Caveney et al.
2006/0223366 A1 10/2006 Murayama et al.

OTHER PUBLICATIONS

International Search Report and Written Opinion for PCT/US2009/0059807, Nov. 17, 2009.

Primary Examiner — Khiem Nguyen

(74) *Attorney, Agent, or Firm* — Timothy M. Morella

(57) **ABSTRACT**

A structure for use with data network management systems uses a plurality of cables interconnecting patch panels, network devices and end-user devices and further utilizes integrated circuits to monitor the status of these end-user devices. The structure includes respective primary (36) and secondary (45) circuit boards. A plurality of connective jacks (31) are mounted on the primary circuit board and these jacks are interconnected to switches and other patch panels within the network. Wires from the jacks extend to and connect with end-user devices and a secondary circuit board is spaced apart from the primary circuit board so as to define a hollow nest (42) within the patch panel assembly that houses and protects integrated circuits (45, 52) and the like.

25 Claims, 19 Drawing Sheets

